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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,157	12/10/2001	Igor Taranov	J141 0002	9698

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EXAMINER	
TRUONG, LAN DAI T	
ART UNIT	**PAPER NUMBER**
2152	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/006,157	TARANOV, IGOR	
	Examiner	Art Unit	
	Lan-Dai Thi Truong	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/23/06;* .
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/08/2006 has been entered.

2. This action is response to communications: application, filed on 12/10/2001; amendment filed 12/08/2006; claims 1-29 are pending; claims 1, 4, 23, 25 are amended; claims 27-29 are added

Response to Arguments

3. The applicant's arguments filed on 12/08/2006 have fully considered but they are moot in view with new ground for rejections

4. In response to applicant's arguments with respect to the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the Tavana teaches away from the use of software for purpose of time stamping) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

5. In response to applicant's arguments with respect to the Tavana fails to show features of applicant's invention e.g. an I/O completion port, wherein the I/O completion port is implemented in an operating system running on a computer; this mended feature is rejected with new ground for rejections by the Silva et al. (U.S. 6,163,805), see the following rejections for details

6. In response to applicant's arguments with respect to the Clark does not teach an I/O completion port implemented in operating system running on a computer; this mended feature is rejected with new ground for rejections by the Silva et al. (U.S. 6,163,805), see the following rejections for details

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or descry bed as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 19 and 21-23 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana et al. (U.S. 2002/0024973) in view of Silva et al. (U.S. 6,163,805)

Regarding claim 1:

Tavana discloses the invention substantially as claimed, including a method, which can be implemented in computer hardware or software code for dispatching bursts of packets onto a computer network, comprising:

Generate a plurality of test packets: (Tavana discloses "test messages" which shares functionality with test packets as claimed is generated and time-stamped for lately sending out to the network: [0040]; abstract, lines 1-13; figure 1; [0002])

Measuring departure time of each of the test packets; and measuring return time of each of the test packets: (Tavana discloses method for marking time-tag for departing time and returning time, then calculating the differences of measured times: abstract, lines 1-13; figure 1; [0002])

Forwarding to the first I/O completion port a request that the test packets be dispatched; dispatching the test packets onto the network using the I/O completion port: (in Tavana's system, test messages are generated and forwarded to "network interface device" which shares functionality with "the first I/O completion port" as claimed; therefrom, the test messages are dispatched into the network: [0034]; [0038]; [0040]; [0019]; [0023]; abstract, lines 1-13; figure 1; [0002])

However, Tavano does not explicitly disclose wherein the I/O completion port implemented in the operating system running on the computer

In analogous art, Silva discloses communications between test requesters, test dispatcher machine and test machines through network interfaces; wherein the test dispatcher machine receives generated test packets and forwards the generated test packets to a suitable test machine: (abstract; column 13, lines 10-67; column 14, lines 1-28; column 8, lines 45-67)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Silva's ideas of interoperating processes of test requesters, test dispatcher machine and test machines through network interfaces with Tavano's system in order to provide efficiency for testing system such as automatically expandable to allow new test machines to be easily and automatically added to the system, and which is distributed such that the users and component of the test system may be distributed over any network, such as Internet, see (Silva: column 2, lines 28-34)

Regarding claim 19:

In addition to rejection in claim 1, Tavana-Silva further discloses Ethernet packets: (Tavana: [0041])

Regarding claim 21:

In addition to rejection in claim 1, Tavana-Silva further discloses receiving returning dispatched test packets after they have traversed a path in the network and time stamping notifications that the packets have been received: (Tavana: abstract, lines 1-13; figure 1; [0002])

Regarding claims 22-23:

Those claims are rejected under rationale of claim 1

Claim 2 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva in view of VanDervort (U.S 5,812,528)

Regarding claim 2:

Tavana-Silva discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein the packets are forwarded to the I/O completion port asynchronously

However, VanDervort discloses a method of measuring "test cell" which is equivalent to "test packets" round trip time within an "ATM communication network " which is shared functionality with "forwardeding to the I/O completion port asynchronously"(abstract: lines 1-16; column 1, lines 23-29)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine VanDervort's ideas of rounding of test cells in an asynchronous transfer mode with Tavana-Silva's system in order to provide flexibility of network configuration and implementation, see (VanDervort: column 2, lines)

Claims 3 and 8-9 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva in view of McKee et al. (U.S. 5,477,531)

Regarding claim 3

Tavana-Silva discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein forwarding the test packets to the I/O completion port is performed by a user mode thread during a single time slice; before forwarding the test packets, terminating the current time slice for the user thread; and forwarding the test packets to the I/O completion port at a start of a next time slice for the user thread

However, McKee discloses a plurality of test packet in one burst are in the same "duration" which is equivalent to 'time slice." McKee also discloses one burst of a plurality of test packets has subsided before the next burst is sent, this process is shared functionality with "forwarding the test packets to the I/O completion port at a start of a next time slice for the user thread": McKee: column 8, lines 40-42; column 9, lines 23-25)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine McKee's ideas of using single time slice to process test packet with Tavana-Silva's system in order to send out sequences of test packets to the target station, see (McKee: column 4, lines 8-12)

Regarding claim 8:

In addition to rejection in claim 3, Tavana-Silva- McKee further discloses returning test packet with time-stamp: (Tavana: [0002])

Regarding claim 9:

This claim is rejected under rationale of claims 3 and 8

Claims 4-7 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva-McKee in view of Madhavapeddi et al. (U.S. 6,975,656)

Regarding claims 4-7:

Tavana-Silva- McKee discloses the invention substantially as disclosed in claim 3, but does not explicitly teach user mode

In analogous art, Madhavapeddi teach user-mode: (column 6, lines 64-67)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Madhavapeddi's ideas of using kernel mode for packets transmissions with Tavana-Silva- McKee's system in order to provide efficiency/ high-resolution for data transmission network, see (Madhavapeddi: abstract)

Claim 11 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva- McKee further in view of Johnson, Jr. (U.S. 5,640,504)

Regarding claim 11:

Tavana-Silva- McKee discloses the invention substantially as disclosed in claim 9, but does not explicitly teach maintaining a private heap for packet data, wherein the private heap is accessible to the user mode thread

However, Johnson discloses method of storing "the receiving information" which is equivalent to "returned test packet" into heap, see (Johnson: column 2, lines 12-19)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson's ideas of using heap for storing test packets with Tavana-Silva- McKee's system in order to routing information see (Johnson: column 2, lines 12-15)

Claim 10 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva-McKee in view of Zhang et al. (U.S. 5,535,193)

Regarding claim 10:

Tavana-Silva-McKee discloses the invention substantially as disclosed in claim 9, but does not explicitly teach counter

In analogous art, Zhang discloses time-stamp counter, see (column 8, lines 29-35)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Zhang's ideas of using time-stamp counter with Tavana-Silva-McKee's system in order to provide an efficient transmitting packets timing measuring system, see (Zhang: abstract)

Claim 17 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva-McKee in view of Williamsom, JR. et al. (U.S. 2003/0084388)

Regarding claim 17:

Tavana-Silva- McKee discloses the invention substantially as disclosed in claim 3, but does not explicitly teach network cards

In analogous art, Williamsom discloses test ports integrated with the card: ([0060]; [0007])

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Williamsom's ideas of using the network card with Tavana-Silva- McKee's system in order to provide convenient/efficiency for test system

Claims 12-16 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva- McKee -Johnson Jr. in view of Garber et al. (U.S. 5,699,539)

Regarding claims 12-14:

Tavana-Silva- McKee -Johnson discloses the invention substantially as disclosed in claim 11, but does not explicitly teach wherein the private heap comprises standard-size allocation units for storing packets; wherein the standard-size allocation units are of an operating system memory page size; wherein the standard-size allocation units are 4096 bytes

However, Garber discloses a heap comprises allocation units for storing data. The allocation unit has size of 4096 bytes, see (Garber: column 1, lines 60-67; column 2, lines 48-54)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Garber's ideas of using heap comprise 4096 bytes allocation units with Tavana-Silva- McKee -Johnson's system in order to provide compressing page, see (Garber: column 2, lines 48-54)

Regarding claims 15-16:

Tavana -Silva- McKee -Johnson discloses the invention substantially as disclosed in claim 11, but does not explicitly teach assigning a larger than default process working set size to the user mode thread; wherein the process working set size exceeds 8 Mbytes.

However, Garber discloses computer system with working set standard size of 8 Mbytes can take care process working set size of 16 Mbytes, see (Garber: column 1, lines 45-50)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Garber's ideas of assigning a larger than default process working set size to the user mode thread with Tavana -Silva- McKee -Johnson's system in order to compress data, see (Garber: abstract, lines 1-27)

Claims 18 and 24 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva further in view of Ranmanathan et al. (U.S 6,076,113)

Regarding claims 18 and 24:

Tavana-Silva discloses the invention substantially as disclosed in claims 1 and 23, but does not explicitly teach wherein generating the test packets comprises generating a plurality of equal-sized test packets

However, Ranmanathan discloses equal size packets to emulate the TCP's transport information, see (Ranmanathan: column 2, lines 33-35)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Ranmanathan's ideas of using equal size packets with Tavana-Silva's system in order to emulate the TCP's transport information, see (Ranmanathan: column 2, lines 33-35)

Claims 27-28 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva in view of Madhavapeddi et al. (U.S. 6,975,656)

Regarding claims 27-28:

Tavana-Silva discloses the invention substantially as disclosed in claims 1 and 23, but does not explicitly teach kernel mode

In analogous art, Madhavapeddi discloses kernel mode for packets transmissions: column 6, lines 1-67; column 7, lines 47-52)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Madhavapeddi's ideas of using kernel mode for packets transmissions with Tavana-Silva's system in order to provide efficiency/ high-resolution for data transmission network, see (Madhavapeddi: abstract)

Claims 25-26 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana et al. (U.S. 2002/0024973) in view of Silva et al. (U.S. 6,163,805) in view of Clark et al. (U.S. 6,075,773) and further in view of McKee et al. (U.S. 5,477,531)

Regarding claim 25:

Tavana discloses the invention substantially as claimed, including a apparatus, which can be implemented in computer hardware or software code for dispatching bursts of packets onto a computer network, comprising:

Establish a first I/O completion port: (Tavana discloses "PHY 24:1" which is equivalent to "a first I/O completion port": abstract, lines 1-13; figure 1; [0002]) or 6163805

Generate a plurality of test packets: (Tavana discloses "an packet" which shares functionality with test packet as claimed is generated and time-stamped for lately sending out to a network: abstract, lines 1-13; figure 1; [0002])

Measuring departure time of each of the test packets; and measuring return time of each of the test packets: (Tavana discloses method for marking time-tag for departing time and returning time them calculating the differences: abstract, lines 1-13; figure 1; [0002])

However, Tavano does not explicitly disclose steps of forwarding to the first I/O completion port a request that the test packets be dispatched, the I/O completion port implemented in the operating system running on the computer; dispatching the test packets onto the network by way of the network interface under control of the first I/O completion port; A network interface

In analogous art, Silva discloses communications between requesters, test dispatcher machine and test machines through network interfaces; wherein the test dispatcher machine receives generated test packets and forwards the generated test packets to suitable test machines: (abstract; column 13, lines 10-67; column 14, lines 1-28; column 8, lines 45-67)

However, Tavano- Silva does not explicitly disclose a computer processor; a program memory accessible to the processor

In analogous art, Clark discloses a packet generating Ethernet testing device comprises "a microprocessor" which is equivalent to "a computer processor;" a packet memory for storing the generated test packets. Clark also discloses the interacting between the processor and packet memory: (abstract, lines 1-20; column 4, lines 45-60)

However, Tavano- Silva-Clark does not explicitly discloses sequencer

In analogous art, McKee discloses "a test sequence program" which is equivalent to "test packet sequencer software" utilizes the services provided by the protocol stack 14 to send a test packet over network. The test sequence program controls the transmission of a test packet to the specified remote station using the protocol stack 14. So it means the test sequence program must receive "request for testing" or command. Then the test packets must be generated and transmits to the destination: (column 3, lines 6-9)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate McKee's ideas of using test sequence program to control transmission test packets and Clark's processor and memory with Tavana-Clark's system in order to provide an efficient packet-based testing system, see (McKee: column 2, lines 7-54)

Regarding claim 26:

This claim is rejected under rationale of claim 25

Claim 29 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva – Clark- McKee in view of Madhavapeddi et al. (U.S. 6,975,656)

Regarding claim 29:

Tavana-Silva – Clark- McKee discloses the invention substantially as disclosed in claims 25, but does not explicitly teach kernel mode

In analogous art, Madhavapeddi discloses kernel mode for packets transmissions: column 6, lines 1-67; column 7, lines 47-52)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Madhavapeddi's ideas of using kernel mode for packets

transmissions with Tavana-Silva – Clark- McKee's system in order to provide efficiency/ high-resolution for data transmission network, see (Madhavapeddi: abstract)

Claim 20 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Silva -Ranmanathan in view of Crayford et al. (U.S. 6,016,308)

Regarding claim 20:

Tavana-Silva -Ranmanathan discloses the invention substantially as disclosed in claim 18, but does not explicitly teach wherein each of the test packets has a size in the range of 46 bytes to 1500 bytes

However, Crayford discloses Ethernet standards packet size is in range of 46 bytes to 1500 bytes, see (Crayford: column 2, lines 6-30)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Crayford's ideas of using packet size in range of 46 bytes to 1548 bytes with Tavana-Silva -Ranmanathan's system in order to indicate a standard frame of data to be sent over the network, see (Crayford: column 2, lines 1-30)

The prior arts made of records and not relied upon are considered pertinent to applicant's disclosure. The following patents and publications are cited to further show the state of the art with respect to "Methods and apparatus for placement of test packets into data communication network": 6163805; 5913073; 4682330; 20020194545; 6502051; 6084944; 7171464 (kernel mode); 6034948 (mode)

Conclusions

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan-Dai Thi Truong whose telephone number is 571-272-7959. The examiner can normally be reached on Monday- Friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob A. Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

02/26/2007